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(54) Low current drive of light emitting device

(57) Control circuitry for an array of light emitting devices (23,27) includes a first column line (20) connected to each light emitting device (23,27) in a column of light emitting devices (23,27). First column circuitry includes a first current source (15) and a second current source (20). The first current source (15) is connected to the first column line (20). The second current source (20) is connected to the first column line (20). When a first light emitting device (23,27) from the column of light emitting devices (23,27) is to be turned on, the first current source (15) is turned on until a voltage on the first column line (20) is equal to a predetermined voltage. Then the first current source (15) is turned off and the second current source (20) supplies current sufficient to cause the first light emitting device (23,27) to emit light to a first brightness level.

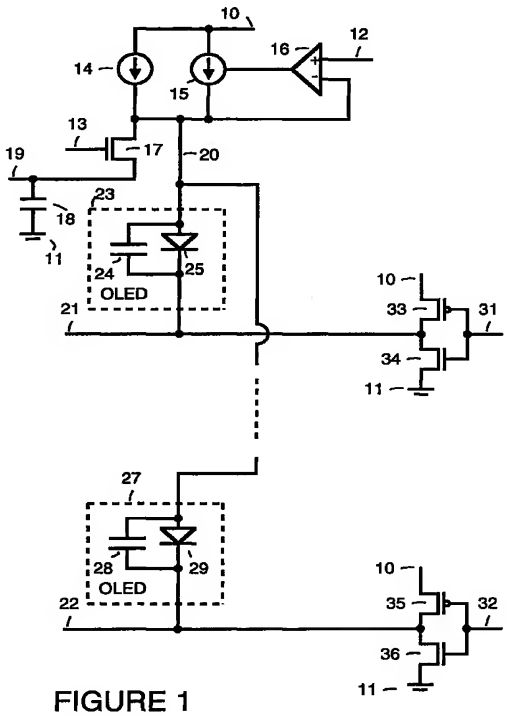

FIGURE 1

EP 1 071 070 A2

Description

BACKGROUND

FIELD OF THE INVENTION

[0001] The present invention pertains to circuitry for driving light emitting devices and pertains particularly to the low current drive of organic light emitting diodes.

RELATED INFORMATION

[0002] The organic light emitting diode (OLED) technology provides a low current emissive display technology. However, a large array of OLEDs contains a large amount of capacitance. This capacitance must be charged and discharged during multiplexed operation.

[0003] An equivalent circuit for an OLED pixel is a capacitor in parallel with the emitting diode. Typically the anodes of each OLED is driven by a current source since the pixel Vf may vary for individual OLEDs across an OLED array.

[0004] A typical implementation of circuitry which drives an array of OLEDs is using current sources to drive a column line for each column of an OLED array. The anode of each OLED is connected to a corresponding column line. The cathodes of each OLED is connected to a corresponding row line of the OLED matrix. Each row line has a switch. The switches enable one row at a time.

[0005] For background information on circuitry for driving OLEDs, see for example, United States Patent Number 5,828,181 issued to Yohiyuki Okuda on October 27, 1998 for DRIVING CIRCUIT FOR AN ORGANIC ELECTROLUMINESCENT ELEMENT USED IN A DISPLAY.

SUMMARY OF THE INVENTION

[0006] In accordance with the preferred embodiment of the present invention, control circuitry for an array of light emitting devices includes a first column line connected to each light emitting device in a column of light emitting devices. First column circuitry includes a first current source and a second current source. The first- current source is connected to the first column line. The second current source is connected to the first column line. When a first light emitting device from the column of light emitting devices is to be turned on, the first current source is turned on until a voltage on the first column line is equal to a predetermined voltage. Then the first current source is turned off and the second current source supplies current sufficient to cause the first light emitting device to emit light to a first brightness level.

[0007] The present invention provides low power operation of a row of light emitting devices. Various embodiments of the invention also allow for reduced complexity when implementing control circuitry for the row of light emitting devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008]

Figure 1 is a schematic which shows circuitry used to drive a light emitting device array in accordance with a preferred embodiment of the present invention.

Figure 2 shows a voltage multiplier used to provide a high voltage for driving the light emitting device array shown in Figure 1.

Figure 3 shows a timing diagram for signals within the light emitting device array shown in Figure 1 in accordance with a preferred embodiment of the present invention.

Figure 4 is a schematic which shows additional circuitry used to drive a light emitting device array in accordance with the preferred embodiment of the present invention.

Figure 5 is a schematic which shows additional circuitry used to drive a light emitting device array in accordance with an alternative preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0009] Figure 1 is a schematic which shows circuitry used to drive an array of light emitting devices. For example, each light emitting device is an organic light emitting diode (OLED) device. A column of light emitting devices is represented by a light emitting device 23 and a light emitting device 27. Light emitting device 23 is the first light emitting device in the column and light emitting device 27 is the last light emitting device in the column. Any number of light emitting devices may be connected within the column between light emitting device 23 and light emitting device 27. A typical array of light emitting devices has 100 columns and 64 rows for a total of 6400 light emitting devices.

[0010] Each light emitting device may be represented by a diode connected in parallel with a capacitance. For example, light emitting device 23 includes a diode 25 and a capacitance 24, connected as shown. Light emitting device 27 includes a diode 29 and a capacitance 28, connected as shown.

[0011] Drive circuitry is used to provide current for each column. The drive circuitry for a column line 20 to which light emitting device 23 and light emitting device 27 are connected consists of a current source 15, a comparator 16, a current source 14 and a transistor 17. For example, current source 14 generates 60 microamps of current. Current source 15 can implemented, for example, as a switch that when turned on connects high pixel voltage line 10 to column line 20.

[0012] A row line is connected to each light emitting

device in a row. Thus row line 21 is connected to all the light emitting devices in the same row as light emitting device 23. Row line 22 is connected to all the light emitting devices in the same row as light emitting device 27. Switches connected to each row line assure that only one row is enabled at a time. Row line 21 is controlled by a switch consisting of a transistor 33 and a transistor 34 connected in an inverter configuration, as shown. The switch is controlled by a switch input 31. Row line 22 is controlled by an switch consisting of a transistor 35 and a transistor 36 connected in an inverter configuration, as shown. The switch is controlled by a switch input 32.

[0013] On high pixel voltage line 10, a voltage is placed sufficient to accommodate the Vf of the light emitting devices. Typically, this is in the range of 8 to 10 volts. On a high logic voltage line 19 a voltage is placed sufficient to accommodate other logic circuitry on the device. Typically, this is in the range of 2.7 to 5 volts. Voltage is measured from a ground 11. A capacitance 18 represents the capacitance of a logic power supply which supplies the high logic voltage. A control input 13 controls switching of transistor 17. The signal on control input 13 is pulse width modulated to allow for brightness control.

[0014] The use of two current sources for each column facilitate implementation of a global brightness control using pulse width modulation. Specifically, while the diode of each light emitting device requires only a low current to generate light, a relatively substantial amount of current is required to charge the capacitance within the light emitting device. If current source 14 is used as a single current source to generate the low amount of current necessary to generate light in a light emitting device, the pixel current generated by current source 14 would take a substantial portion of the time that each row is enabled to charge the column to the required activation voltage (Vf) of an active light emitting device. Pulse width modulation of the signal on control input 13 results in even less current being available to charge the column.

[0015] The addition of large current source 15 provides a lot of current at the beginning of each column cycle to charge the column to a predetermined voltage. During the charging period, a reference voltage equivalent to the predetermined voltage is placed on a reference voltage line 12. Once the predetermined voltage is reached, comparator 16 shuts off current source 15. Current source 15, then, provides a "fast charge" current to charge the capacitance of the active light emitting device in the column before allowing current source 14 to take over and supply the desired pixel current. This allows current source 14 to provide sufficient current to cause an activated light emitting device to generate light for a substantial portion of the column cycle. This enables predictable brightness control with pulse width modulation.

[0016] A typical low power application has a logic power supply of 2.7 volts to 5 volts. An light emitting device, however, typically requires 8 volts to 10 volts to accommodate the Vf of the light emitting device. Thus to generate a high voltage to place on a high voltage line 10, a voltage multiplier is used.

[0017] Figure 2 shows a voltage multiplier including a resistor 41, a resistor 42 a comparator 44 an oscillator 45, an inverter 46 a transistor 48, an inductor 49, a diode 51 and a capacitor 52 connected as shown.

[0018] For example, resistor 41 has a value of 62 kilohms. Resistor 42 has a value of 455 kilohms. Inductor 49 has a value of 22 microhenries. Capacitor 52 has a value of 10 microfarads. Diode 51 is a Schottky diode. When not disabled by a signal from comparator 44, oscillator 45 generates a signal having a frequency of 60 kilohertz. A reference voltage of 1.2 volts is placed on a reference voltage line 43. A ground line 11 is at 0 volts. On high logic voltage line 19, a voltage of 2.7 volts is placed. The voltage multiplier places a 10 voltage DC signal on high pixel voltage line 10. The DC signal on high pixel voltage line 10 is stored in capacitor 52.

[0019] Figure 3 shows a simplified timing diagram which explains the operation of the circuitry shown in Figure 1. A waveform 61 represents the signal on a row line for a row "n". For example, row "n" represents the row which contains light emitting device 23. Therefore, waveform 61 represents the signal on row line 21. A waveform 62 represents the signal on a row line for a row "n+1". A waveform 63 represents the signal on a row line for a row "n+2". A waveform 64 represents the signal on a row line for a row "n+3". A waveform 65 represents the signal on a row line for a row "n+4".

[0020] A waveform 66 represents a signal placed on column line 20. Column data 67 indicates whether a light emitting device in an activated row will be on or off during a particular time period. "ON" indicates that a light emitting device in the column is to be turned on. "OFF" indicates that no light emitting device in the column is to be turned on.

[0021] At most, only one light emitting device is turned on at a time for each column. In order for a light emitting device to be turned on, the voltage on the column line connected to the light emitting device must be at Vf (e.g., 6 to 8 volts) or greater and the voltage on the row line must be at low voltage (e.g., 0 volts) . Thus for light emitting device 23 to be turned on, column line 20 must be at Vf or greater (e.g., 6 to 8 volts) and row line 21 must be at low voltage (e.g., 0 volts). For light emitting device 27 to be turned on, column line 20 must be at Vf or greater (e.g., 6 to 8 volts) and row line 22 must be at low voltage (e.g., 0 volts).

[0022] The times that the row lines are brought to low voltage are staggered , so that at most only one light emitting device is turned on at a time for each column. Thus, at a time period 71, the row line for row n (i.e., row line 21) is at low voltage. All other rows remain at high voltage. At a time period 72, the row line for row n+1 is at low voltage. All other rows remain at high voltage. At

a time period 73, the row line for row n+2 is at low voltage. All other rows remain at high voltage. At a time period 74, the row line for row n+3 is at low voltage. All other rows remain at high voltage. At a time period 75, the row line for row n+4 is at low voltage. All other rows remain at high voltage.

[0023] In order for the column charge time to be independent of the previous state of the array of light emitting devices, at the beginning of each column cycle, all the row lines are at the high voltage and all the column lines, including those that were turned on in the previous column cycle, are placed at the column low voltage. As a result of this, all light emitting devices are reverse biased at the beginning of a new column cycle. This is illustrated in Figure 3 by waveform 66 being at column low voltage (e.g. 2.7 volts) between time period 71 and time period 72, between time period 72 and time period 73, between time period 73 and time period 74 and between time period 74 and time period 75.

[0024] For each column, during the time period when each row line is brought to low voltage, if the light emitting device for that column connected to that row line is to be turned on, the column line is brought to Vf or greater. Otherwise, the column line is left at column low voltage.

[0025] For example, in time period 71, the light emitting device (i.e., light emitting device 23) in row n (i.e., connected to row line 21) is to be turned on. Therefore, in time period 71, column 20 is driven to a voltage that is equal to or greater than Vf. In time period 72, the light emitting device in row n+1 is to be turned on. Therefore, in time period 72, column 20 is driven to a voltage that is equal to or greater than Vf. In time period 73, the light emitting device in row n+2 is to be turned off. Therefore, in time period 73, column 20 remains at column low voltage. In time period 74, the light emitting device in row n+3 is to be turned on. Therefore, in time period 74, column 20 is driven to a voltage that is equal to or greater than Vf. In time period 75, the light emitting device in row n+4 is to be turned off. Therefore, in time period 75, column 20 remains at column low voltage.

[0026] When column line 20 is at Vf or greater, one row line is switched to the low voltage and all the other row lines are switched to the high voltage. This reduces the current actually drawn from the power supply. For example, when light emitting device 23 is turned off, transistor 31 connects row line 21 to high voltage line 10. Any current that travels through light emitting device 21 travels to high voltage line 10 and back into capacitor 52 of the high voltage multiplier shown in Figure 2.

[0027] When light emitting device 23 is turned on, column line 20 is at the Vf or greater and row line 21 is connected to ground 11. This results in charging capacitance 24. Once the voltage across capacitance 24 is greater than Vf, diode 25 generates light. Any current that travels through the capacitance of other light emitting devices in the column travels to high voltage line 10 and back into capacitor 52 of the high voltage multiplier shown in Figure 2.

[0028] In the preferred embodiment, column low voltage is at 2.7 volts. This is equivalent to the logic high voltage for logic circuitry. The reason this is done is because the logic power supply supplied voltage of 2.7 volts is below the minimum Vf required to turn on a light emitting device. When a column makes a transition from Vf or greater to column low voltage, charge remains in the capacitance for the light emitting device that was "on" and to a lesser degree in capacitance for other light emitting devices. This charge is used to charge the capacitance of the logic voltage supply.

[0029] For example, in time period 71, light emitting device 23 is turned on. At the end of time period 72, transistor 17 is turned on and column line 20 is electrically connected through high logic voltage line 19 to capacitance 18 of the logic power supply. Capacitance 24 thus discharges into capacitance 18.

[0030] While in the preferred embodiment, at the beginning of each column cycle, the column lines that were turned on in the previous column cycle are driven low. In an alternate embodiment of the present invention, further reduction of the column charge and discharge currents is achieved by logically detecting that a column line has been on during activation of one row line and will remain on during activation of the next row line. When this case is detected, column line is not discharged, but remains at Vf. In this embodiment, waveform 66, shown in Figure 3, would remain at Vf between time period 71 and time period 72. Waveform 66 would still be at column low voltage (e.g. 2.7 volts) between time period between time period 72 and time period 73, between time period 73 and time period 74 and between time period 74 and time period 75.

[0031] Also, in the preferred embodiment a comparator is tied to a high current supply for each column. Thus there are as many comparators as there are columns. In an alternative embodiment of the present invention, instead of using a separate comparator to monitor each column of the array, only one comparator is used. This single comparator is tied to a current source and capacitor which mirrors the fast charge current and column capacitance. This is illustrated by Figures 4 and 5.

[0032] Figure 4 illustrates the preferred embodiment. In the preferred embodiment a comparator is tied to a high current supply for each column. Thus driving circuitry for column line 20 includes pulse modulated current source 14, high current source 15 and comparator 16. The driving circuitry for a column line 120 includes a pulse modulated current source 114, a high current source 115 and a comparator 116.

[0033] Figure 5 illustrates the alternative embodiment. In the alternative embodiment only comparator 216 is used. Comparator 216 is tied to a current source 215 and a capacitor 221. Current source 215 and a capacitor 221 mirror the fast charge current and column capacitance. Comparator 216 is used to control high

current source 15 connected to column line 20, and to control high current source 115 connected to column line 120. Comparator 16 and comparator 116 are no longer required.

[0034] In the above description of the preferred embodiment, circuitry that controls an array of organic light emitting diodes is described. However, as will be understood by a person of ordinary skill in the art, the above described circuitry can be used with great benefit to drive an array of any type of light emitting device in which there is some capacitance which is charged before a light emitting device turns on.

Claims

1. Control circuitry for an array of light emitting devices (23,27), circuitry comprising:

   a first column line (20) connected to each light emitting device (23,27) in a column of light emitting devices (23,27);
   first column circuitry comprising:

   a first current source (15) connected to the first column line (20), and
   a second current source (20) connected to the first column line (20) ;

   wherein when a first light emitting device (23,27) from the column of light emitting devices (23,27) is to be turned on, the first current source (15) is turned on until a voltage on the first column line (20) is equal to a predetermined voltage, then the first current source (15) is turned off and the second current source (20) supplies current sufficient to cause the first light emitting device (23,27) to emit light to a first brightness level.

2. Control circuitry as in claim 1, wherein the first column circuitry additionally comprises:

   a switch (17) connected to the first column line (20) and to an output capacitance (18) of a low voltage power supply;
   wherein when the voltage on the first column line (20) is to be discharged, the switch (17) is turned on allowing the voltage to be discharged to the output capacitance (18) of the low voltage power supply.

3. Control circuitry as in any previous claim additionally comprising:.

   a second column line (120);
   second column circuitry comprising:

   a third current source (115) connected to the second column line (120), and
   a fourth current source (114) connected to the second column line (120).

4. Control circuitry as in claim 3 additionally comprising:

   a capacitance (221);
   a fifth current source (215) which charges the capacitance (221),
   a comparator (216) which compares a reference voltage on a reference voltage line (12) to a voltage across the capacitance (221), the comparator (216) controlling the first current source (15), the third current source (115) and the fifth current source (215)
   wherein the comparator (216) turns off the first current source (15) when the voltage across the capacitance (221) is equal to the reference voltage.

5. Control circuitry as in any previous claim additionally comprising:

   a power supply having an output on which is placed a signal with a voltage high enough to turn on light emitting devices (23,27) from the array of light emitting devices (23,27);
   a plurality of row lines (21,22) ;
   a plurality of switches (33-36), each switch (33-36) connected to an associated row line from the plurality of row Lines (21,22), each switch (33-36) connecting the associated row line (21,22) to either the output of the power supply (10) or to ground (11).

6. A method for controlling an array of light emitting devices (23,27), circuitry comprising the following steps:

   (a) when a first light emitting device (23,27) from a column of light emitting devices (23,27) is to be turned on, charging capacitance (24,28) of the first light emitting diode (23,27) utilizing a first current source (15) until a voltage across the first light emitting device (23,27) is equal to a predetermined voltage;
   (b) when the voltage across the first light emitting device (23,27) is equal to the predetermined voltage, shutting off the first current source (15); and,
   (c) utilizing a second current source (20) to supply current sufficient to cause the first light emitting device (23,27) to emit light to a first brightness level.

7. A method as in claim 6, additionally comprising the following step:

(d) when the first light emitting device (23,27) is to be turned off, discharging the capacitance (24,28) of the first light emitting device (23,27) to output capacitance (18) of a low voltage power supply.

8. A method as in claim 6 or 7, wherein step (a) includes the following substeps:

(a.2) while charging the capacitance (24,28) of the first light emitting device (23,27) also charging a mirror capacitance (221) using a third current source (215);
(a.1) comparing a reference voltage on a reference voltage line (12) to the voltage across the mirror capacitance (221).

9. A method as in claim 6, 7 or 8 additionally comprising the following step:

(d) when the first light emitting device (23,27) is turned off, reverse biasing the first light emitting device (23,27) such that charge stored in the light emitting device (23,27) flows back into a capacitor (18) on a voltage supply.

10. A method as in claim 6, 7, 8 or 9 wherein the array of light emitting devices (23,27) is an array of organic light emitting diodes.

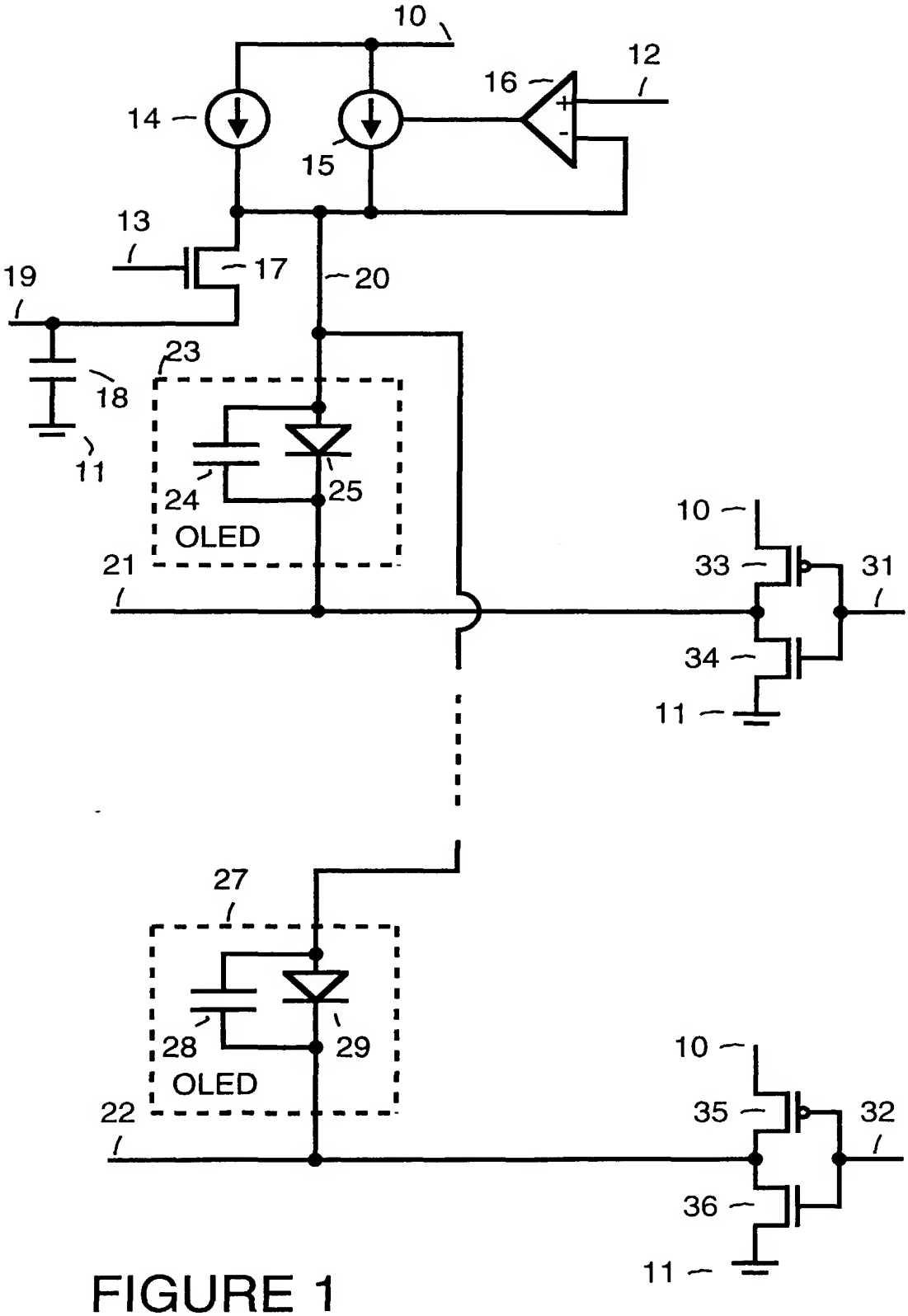
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FIGURE 1

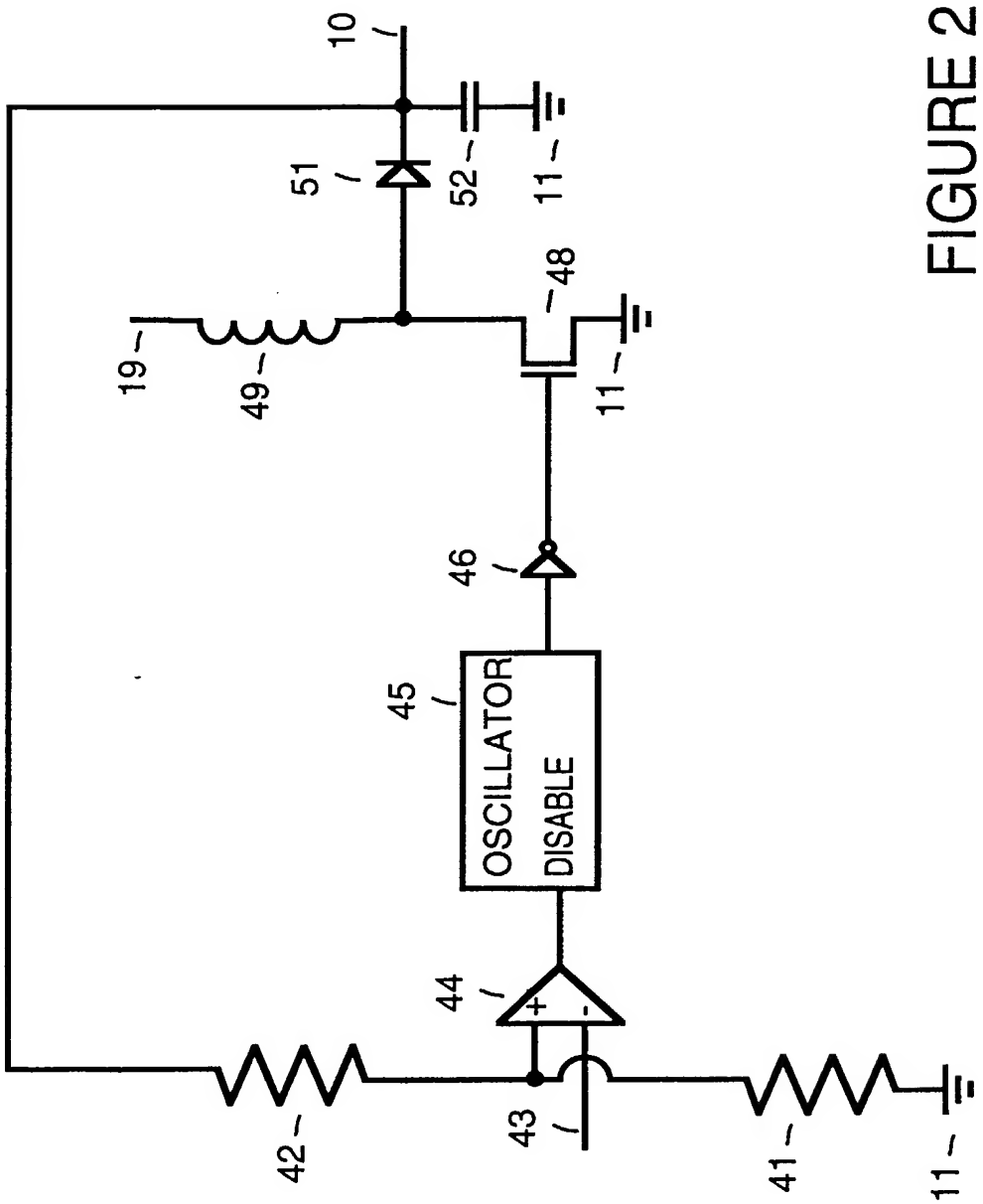
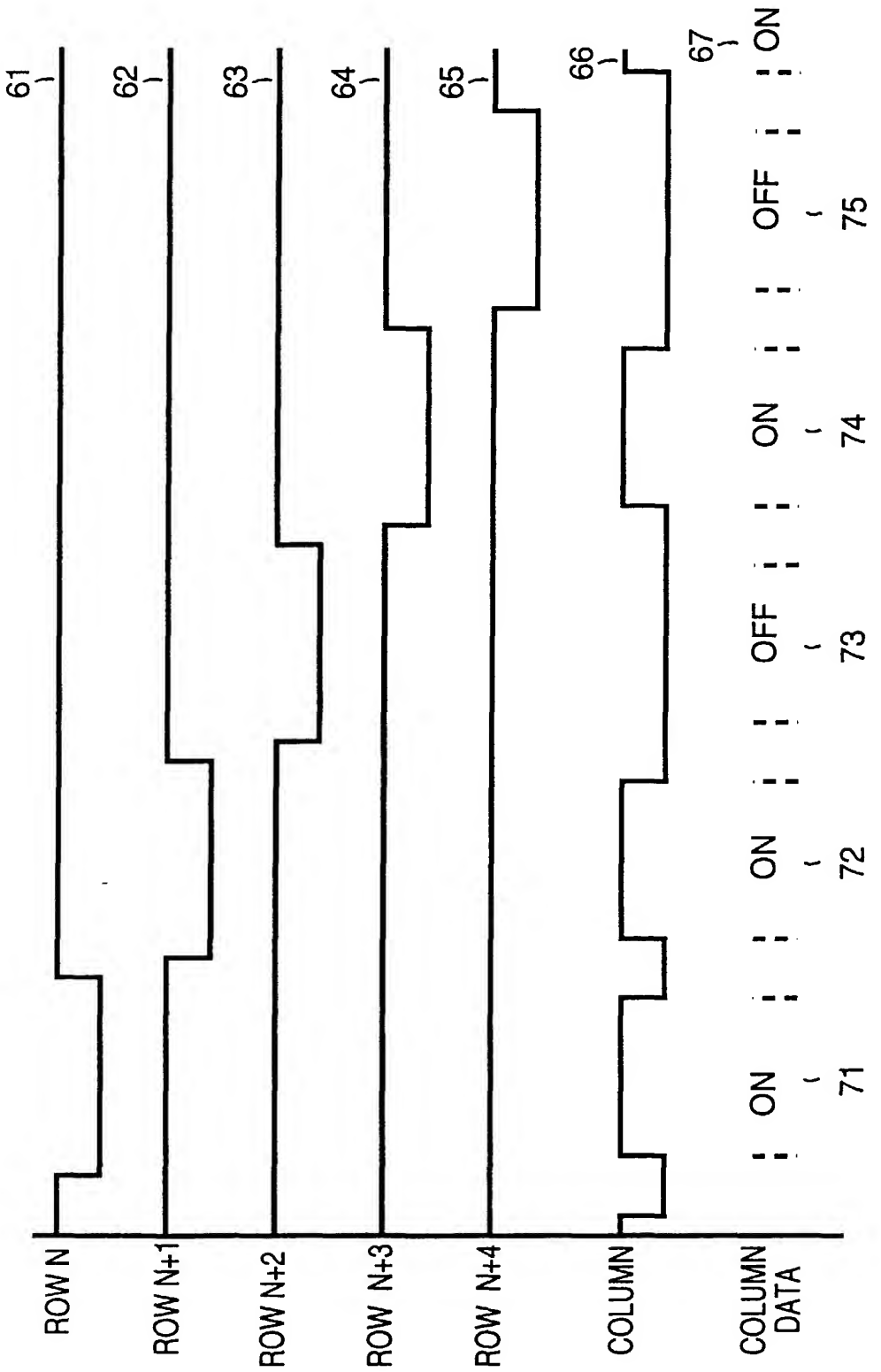


FIGURE 2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COLUMN
COLUMN DATA

FIGURE 3

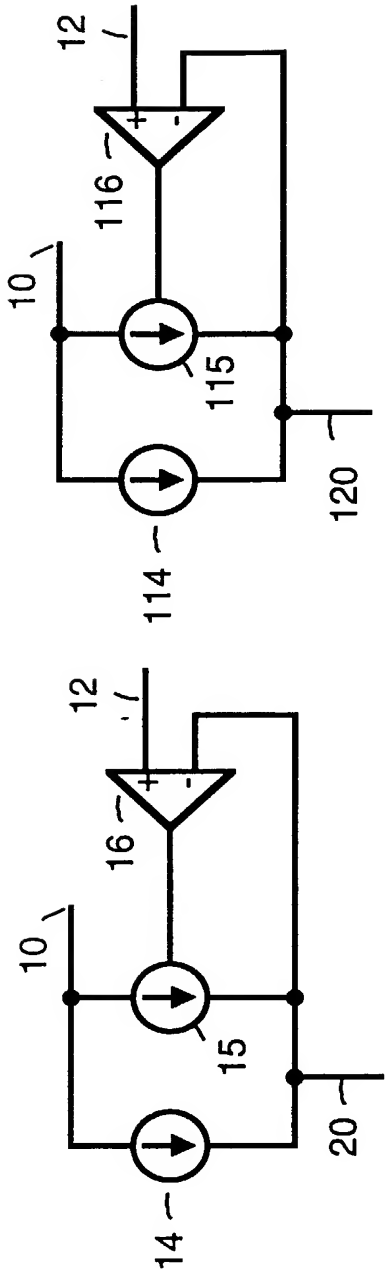

FIGURE 4

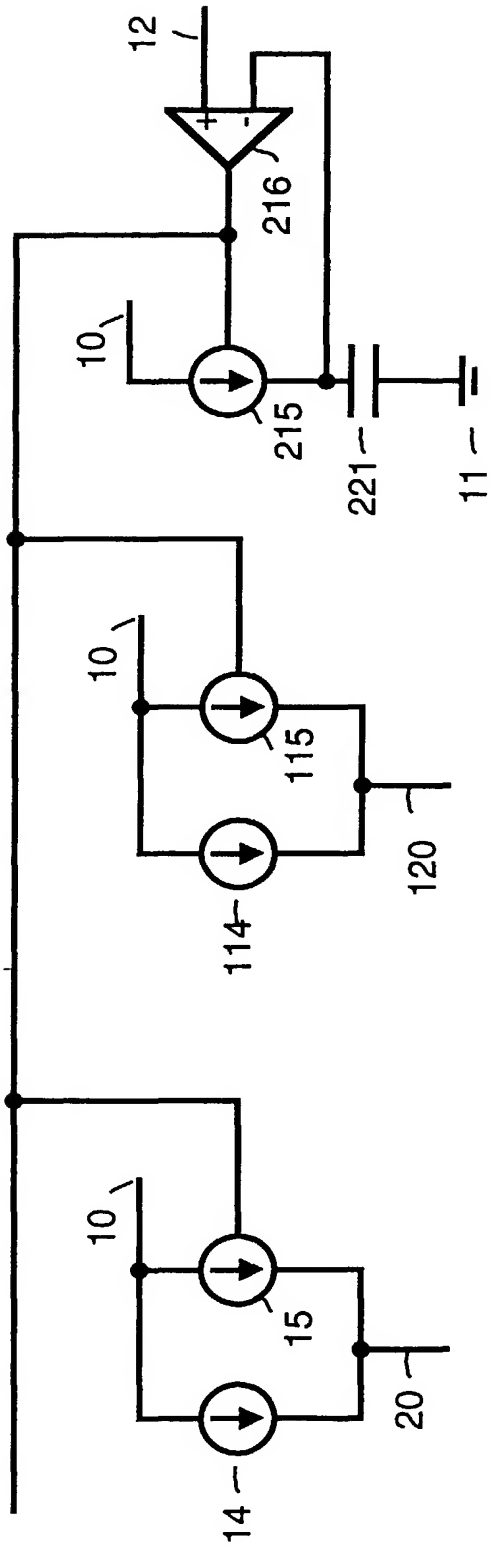

FIGURE 5

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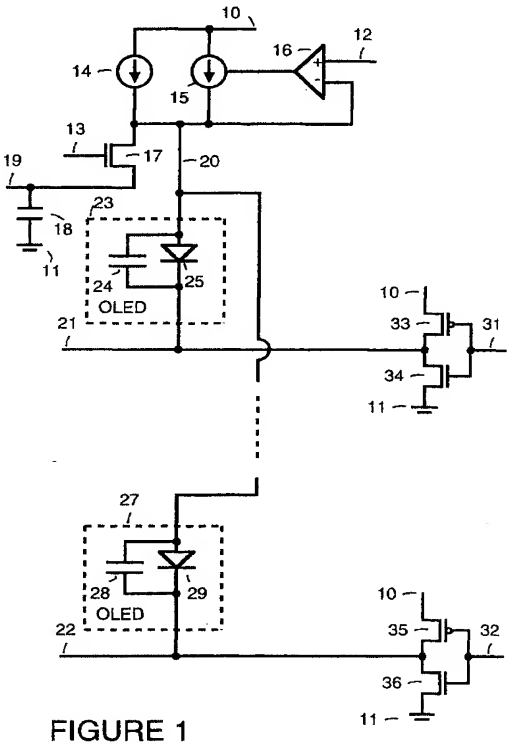

FIGURE 1

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 11 2843

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 552 677 A (PAGONES ANDREW) 3 September 1996 (1996-09-03) * column 2, line 12 - column 3, line 55; figures 1,2 *	1,3,6	G09G3/32
A	* column 4, line 6 - column 4, line 17 *	1-10	
X	US 4 366 504 A (KANATANI YOSHIHARU) 28 December 1982 (1982-12-28) * column 2, line 42 - column 4, line 44; figures 2,3 *	1,6	
A	* column 4, line 46 - column 6, line 9 *	1-10	
Y	US 5 923 309 A (ISHIZUKA SHINICHI ET AL) 13 July 1999 (1999-07-13) * column 5, line 7 - column 7, line 16; figure 8 *	1,3	
A	* column 3, line 19 - column 4, line 21; figures 2-4 *	1-10	
Y	US 5 684 368 A (SO FRANKY ET AL) 4 November 1997 (1997-11-04)	1,3	
A	* column 5, line 66 - column 6, line 65; figures 4,5 *	4,5	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G09G
A	US 5 723 950 A (SO FRANKY ET AL) 3 March 1998 (1998-03-03) * column 5, line 14 - column 6, line 2; figures 3,4 *	1,6,10	
A	EP 0 784 305 A (MOTOROLA INC) 16 July 1997 (1997-07-16) * column 9, line 15 - column 9, line 51; figure 3 *	1-10	
A	US 5 923 308 A (KIM MATTHEW ET AL) 13 July 1999 (1999-07-13) * column 3, line 4 - column 4, line 11; figures 1,2 *	1-10	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	19 November 2001	Morris, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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A	US 5 847 516 A (HATTORI TADASHI ET AL) 8 December 1998 (1998-12-08) * column 11, line 30 - column 12, line 41; figure 13 *	2	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

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Place of search	Date of completion of the search	Examiner
MUNICH	19 November 2001	Morris, D

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5552677 A	03-09-1996	FR 2733852 A1	08-11-1996
		JP 8305318 A	22-11-1996
US 4366504 A	28-12-1982	JP 1345249 C	29-10-1986
		JP 54159817 A	18-12-1979
		JP 61009790 B	26-03-1986
		JP 1290691 C	29-11-1985
		JP 54053982 A	27-04-1979
		JP 60015079 B	17-04-1985
		JP 1319124 C	29-05-1986
		JP 54055118 A	02-05-1979
		JP 60044869 B	05-10-1985
		DE 2843801 A1	19-04-1979
		FR 2405604 A1	04-05-1979
		GB 2008303 A ,B	31-05-1979
		GB 2057743 A ,B	01-04-1981
US 5923309 A	13-07-1999	JP 9305146 A	28-11-1997
US 5684368 A	04-11-1997	EP 0813180 A1	17-12-1997
		JP 10063228 A	06-03-1998
US 5723950 A	03-03-1998	NONE	
EP 0784305 A	16-07-1997	US 5719589 A	17-02-1998
		EP 0784305 A1	16-07-1997
		JP 9281902 A	31-10-1997
US 5923308 A	13-07-1999	NONE	
US 5847516 A	08-12-1998	JP 2897695 B2	31-05-1999
		JP 9054565 A	25-02-1997
		JP 2914234 B2	28-06-1999
		JP 9054566 A	25-02-1997
		JP 3039378 B2	08-05-2000
		JP 9073282 A	18-03-1997
		US 6064158 A	16-05-2000
		US 6121943 A	19-09-2000

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82